IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: KASPER	Examiner: P. Nguyen
Serial No. 09/163,925	
Filing Date: September 30, 1998	Art Unit: 2665
Confirmation No. 6051	
For: METHOD AND SYSTEM OF ROUTING NETWORK-BASED DATA USING FRAME ADDRESS NOTIFICATION	

DECLARATION UNDER 37 CFR 1.131

Director, U.S. Patent and Trademark Office
Washington, DC 20231

Sir:

Christian D. Kasper hereby declares:

1. I am the inventor of Claims 1-42 of the patent application identified above and the inventor of the subject matter described and claimed therein.

2. Prior to June 19, 1998, the effective date of the cited U.S. Patent No. 6,195,720 to Abiven et al., I conceived and reduced to practice the invention as described and claimed in the subject application in this country at the SGS-Thomson Microelectronics, Inc. (now STMicroelectronics, Inc.) plant in Carrollton, Texas.

3. Attached hereto is Exhibit 1 with sheets 1-17 as evidence of my conception and reduction to practice of the invention.

4. As noted in the attached sheets 1-17 of Exhibit 1, I originally conceived the invention of using a frame address notification as a signal interrupt to the host CPU such that all relevant address fields for a received frame were currently resident in memory. The frame could be processed by the address and look-up engine (ALE) and dispatched to its destination to provide a pipelining effect that allows routing to occur in parallel, while the remainder of the frame could still be incoming off the network wire. The DMA burst-size could be selected and cause appropriate address fields to be a variable within the initial burst read of the frame. Any MAC-level header, IP addresses, or even TCP/UDP ports could be read into memory by having the CPA look into an incoming frame for routing. This overcame the drawbacks of classic store and forward (SF) architecture where the host device was obligated to wait until the entire frame had been read off the wire and ownership of the associated external memory buffer had been reassigned before routing could take place.

5. Sheets 1-7 show the basic method and system with the FIFO receive memory, network device, host processor, shared system memory and direct memory access unit as part of an HDLC device. The communications processor selects the amount of data to be transferred from the FIFO receive memory to the shared system memory based on the desired address field to be analyzed by the host processor.

6. Sheets 8-11 show different headers and a TCP/UDP datagram encapsulated in an IP and MAC layer frame as examples of headers that could be used in the present invention.

7. Sheets 12-17 further show my write-up and various notes setting forth basic aspects of the invention.

8. Sheets 15 and 16 show the receive interrupt event time line and frame address notification of the present invention with the DMA interrupts, respectively.

9. Sheet 17 shows the type of device in which I implemented firmware for the present invention. That device was a four port, 32-bit, controller produced by STMicroelectronics as a SWIFT™ ST52T3 fast HDLC controller.

10. Each of the dates deleted from the sheets of Exhibit A are prior to June 19, 1998.

I hereby declare that all statements made herein are of my own knowledge are true and that all statements made on information and belief are true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

7/29/2
Date

w/Kasper
CHRISTIAN D. KASPER

HDLC Packet Reception Example (Slide #1)

Initial Block Diagram

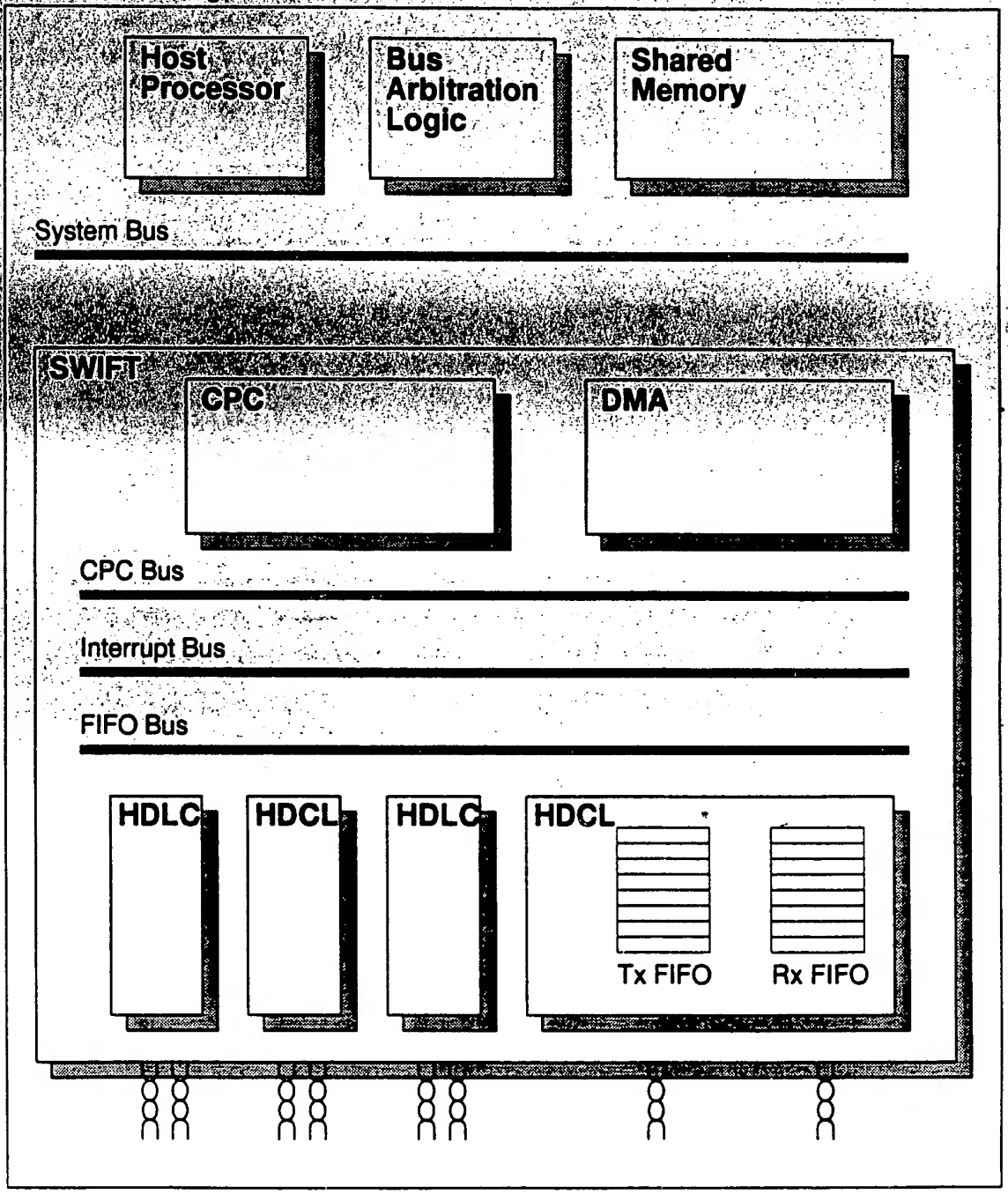
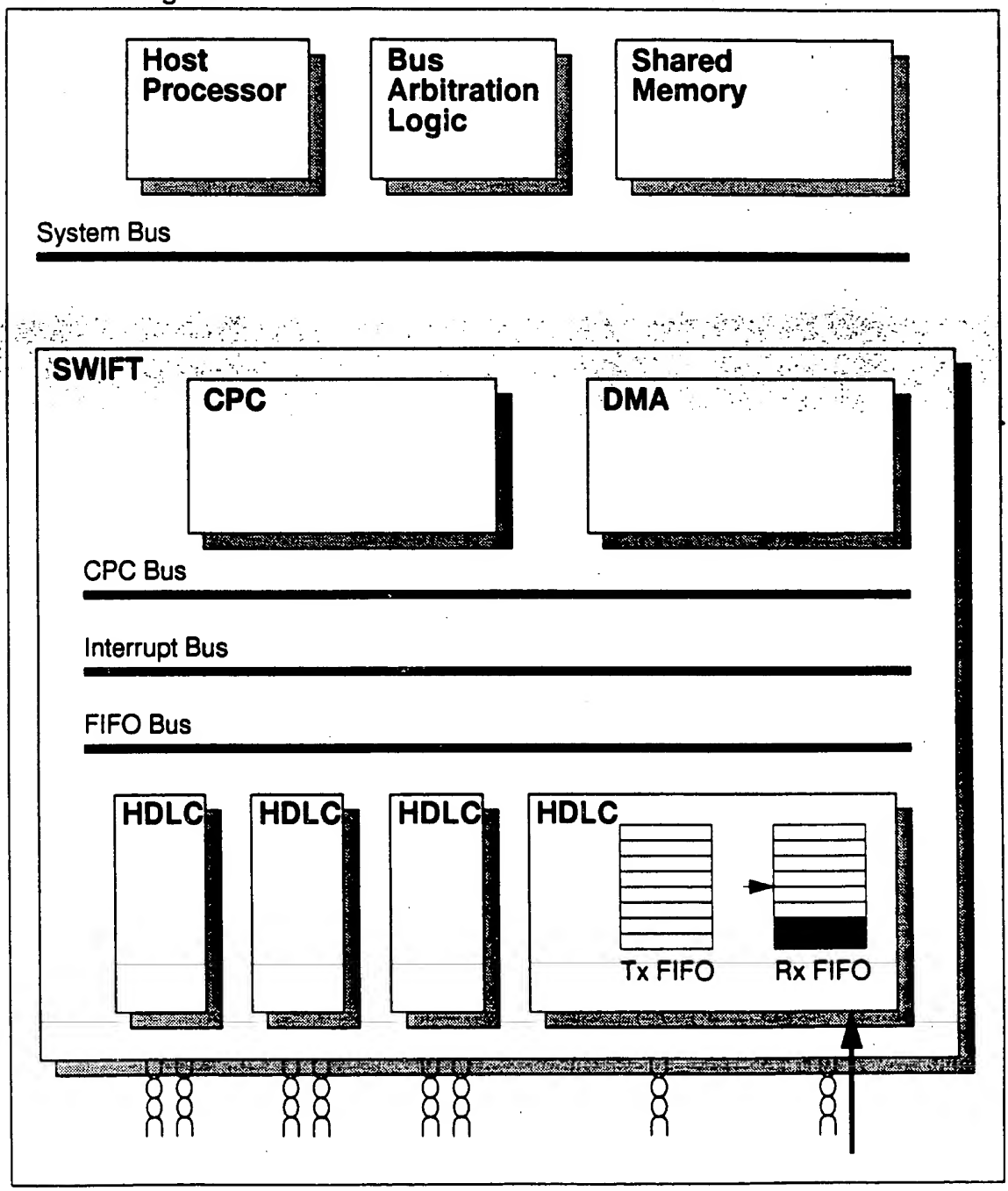


EXHIBIT 1

1

HDLC Packet Reception Example (Slide #2)

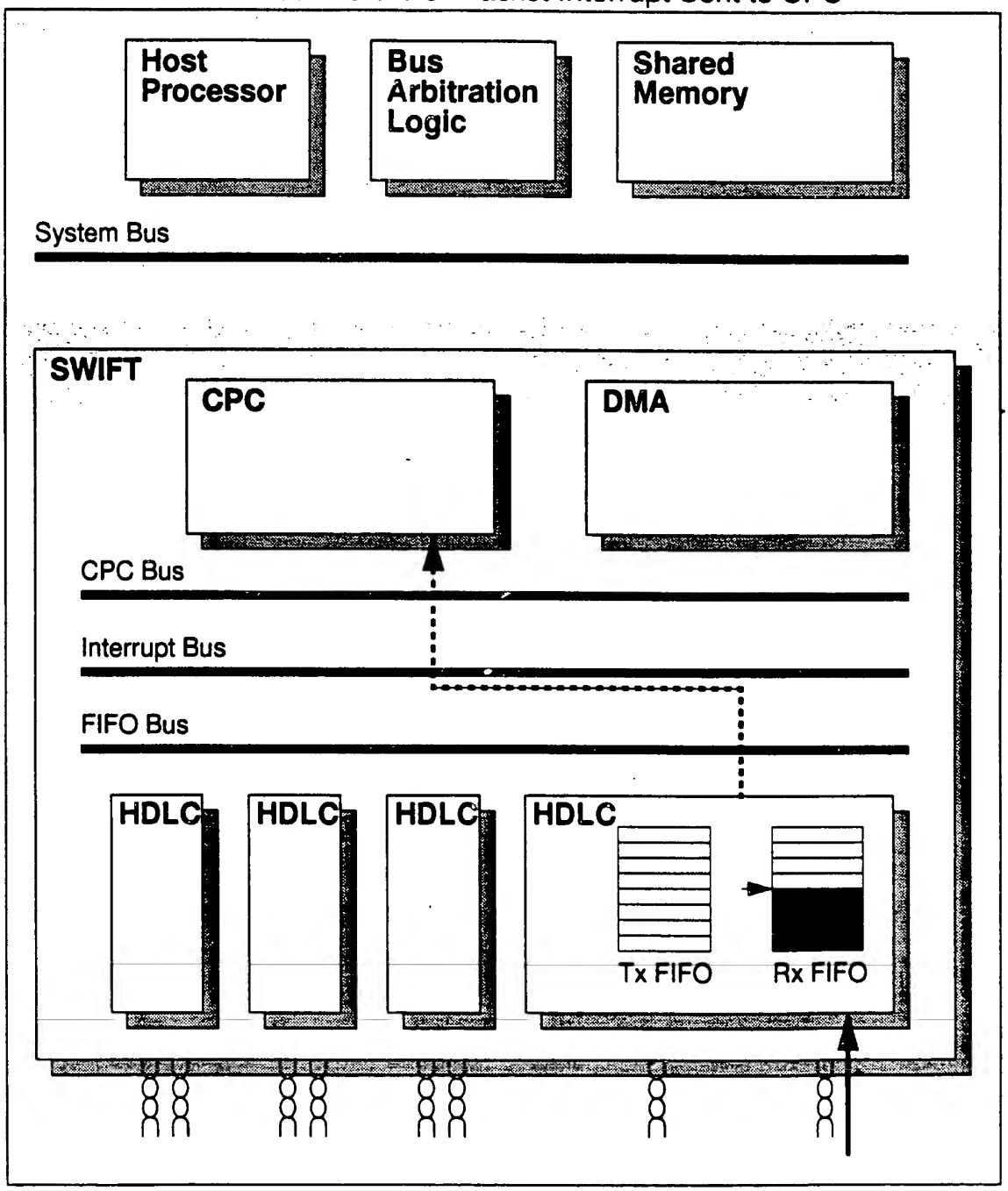
Rx FIFO Begins to Fill with a New Packet



2

HDLC Packet Reception Example (Slide #3)

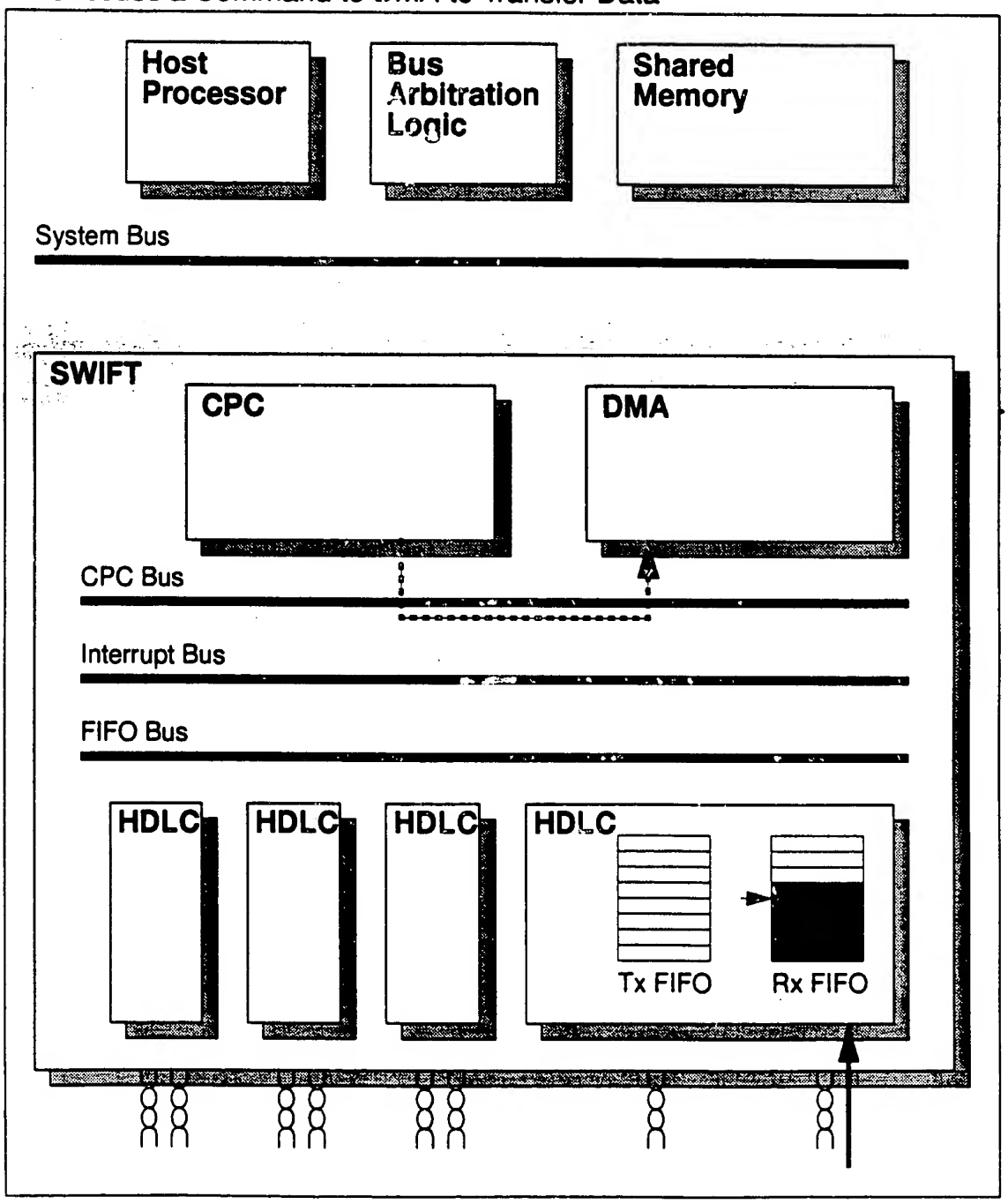
Rx Threshold Reached – Start-Of-Packet Interrupt Sent to CPC



3

HDLC Packet Reception Example (Slide #4)

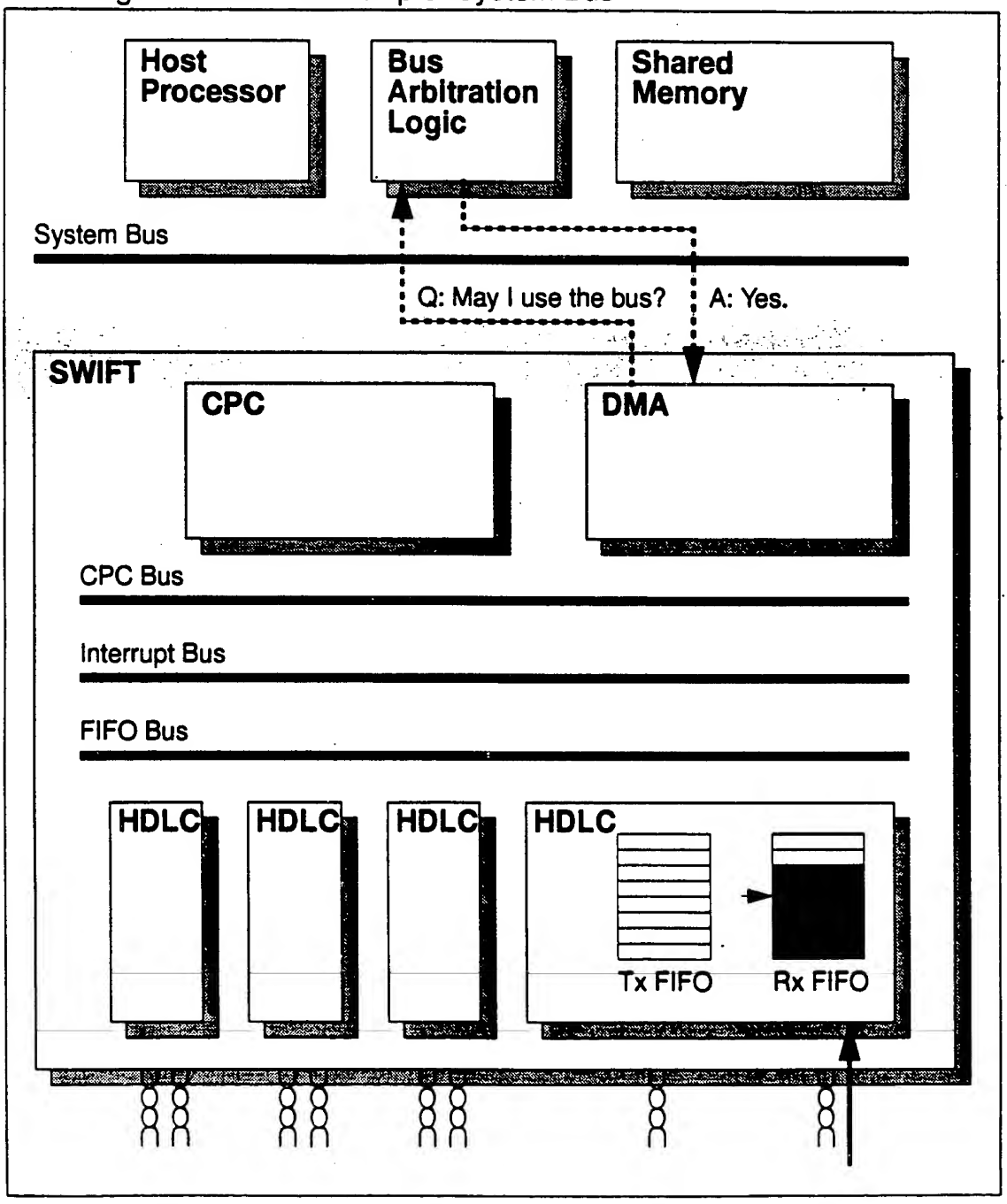
CPC Issues a Command to DMA to Transfer Data



4

HDLC Packet Reception Example (Slide #5)

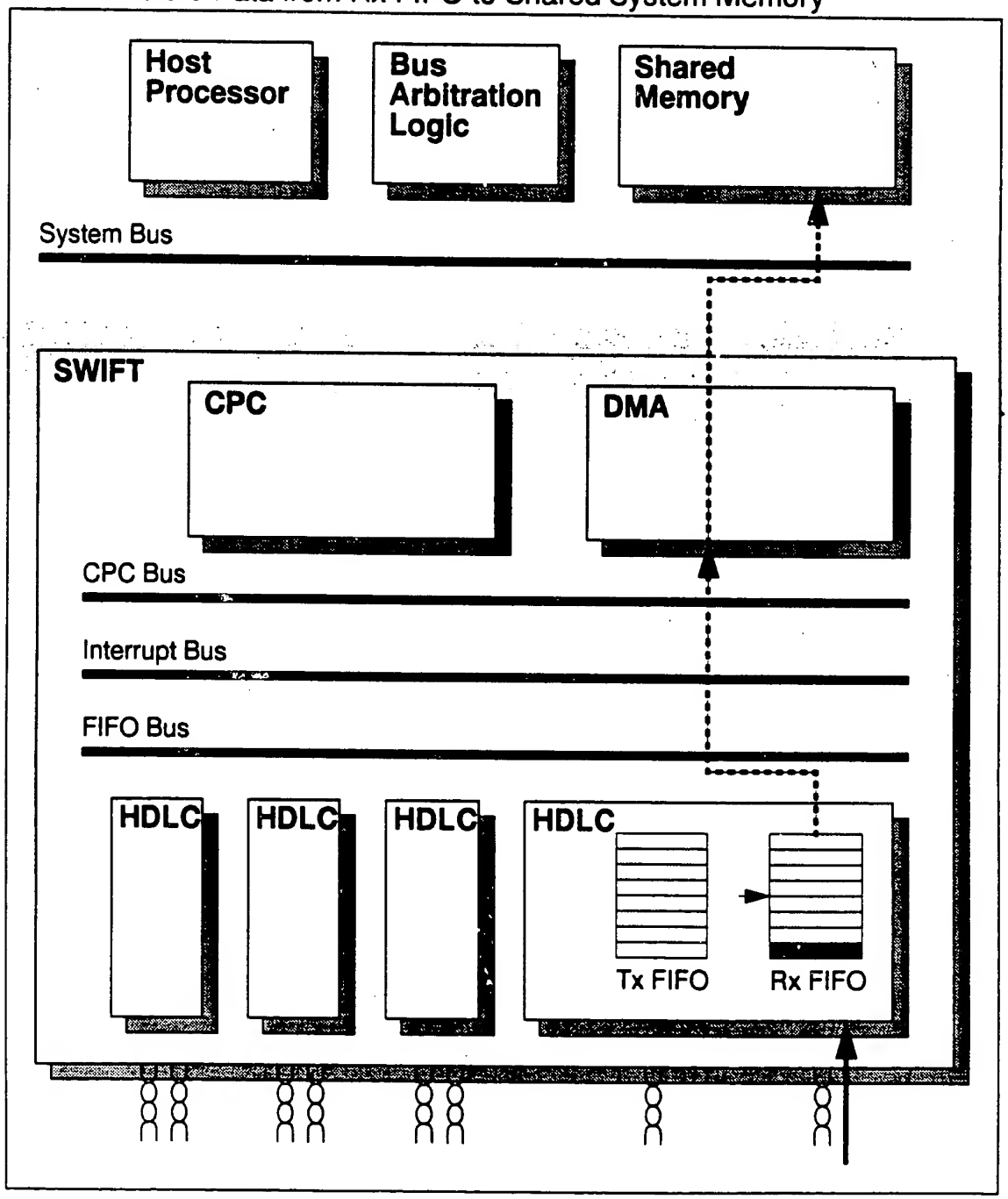
DMA Negotiates for Ownership of System Bus



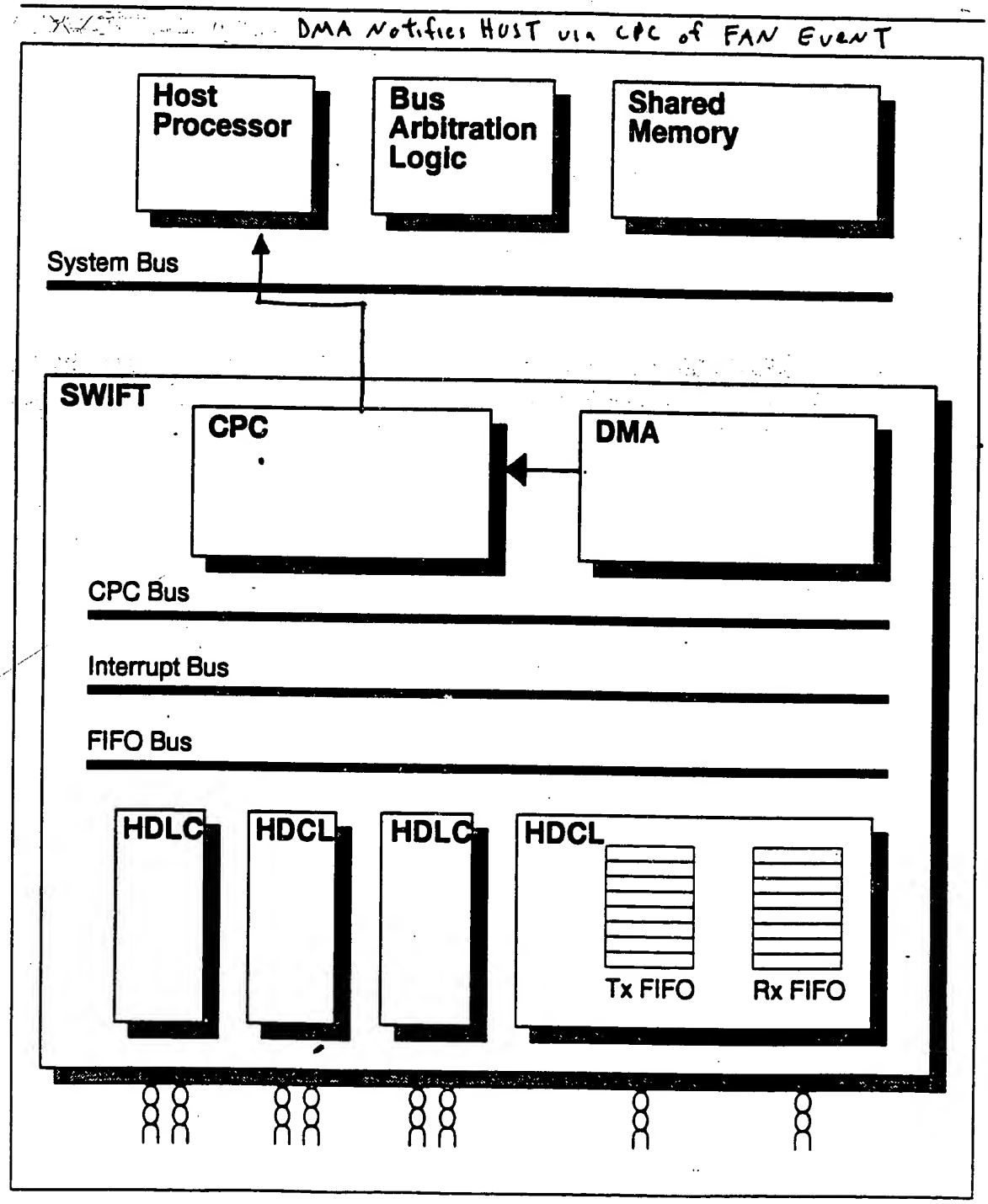
5

HDLC Packet Reception Example (Slide #6)

DMA Transfers Data from Rx FIFO to Shared System Memory



HDLC Packet Reception Example (Slide #7)



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TCP HEADER (20 BYTES)

Table 1:

16-BIT SOURCE PORT	16-BIT DESTINATION PORT
32-BIT SEQUENCE NUMBER	
32-BIT ACKNOWLEDGMENT NUMBER	
URG/ACK/PSH/RST/SYN/FIN	16-BIT WINDOW SIZE
16-BIT TCP CHECKSUM	16-BIT URGENT POINTER

FILE: ~/patents/FAN/tcp.header.fm5

SGS-THOMSON Microelectronics, Inc. - 1310 Electronics Drive. - Carrollton, TX 75006-5039
Telephone (214) 466-6000, Telex 730643

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MICROELECTRONICS

INTERNET IP HEADER (20 Bytes)

Table 1:

VER/HEADER	TYPE OF SERVICE	16-BIT TOTAL LENGTH (IN BYTES)
16-BIT IDENTIFICATON		3-BIT FLAGS/13-BIT FRAGMENT OFFSET
TTL	8-BIT PROTOCOL	16-BIT HEADER CHECKSUM
32-BIT SOURCE IP ADDRESS		
32-BIT DESTINATION IP ADDRESS		
(OPTIONS - IF ANY)		

~/PATENTS/FAN/ip.header.fm5

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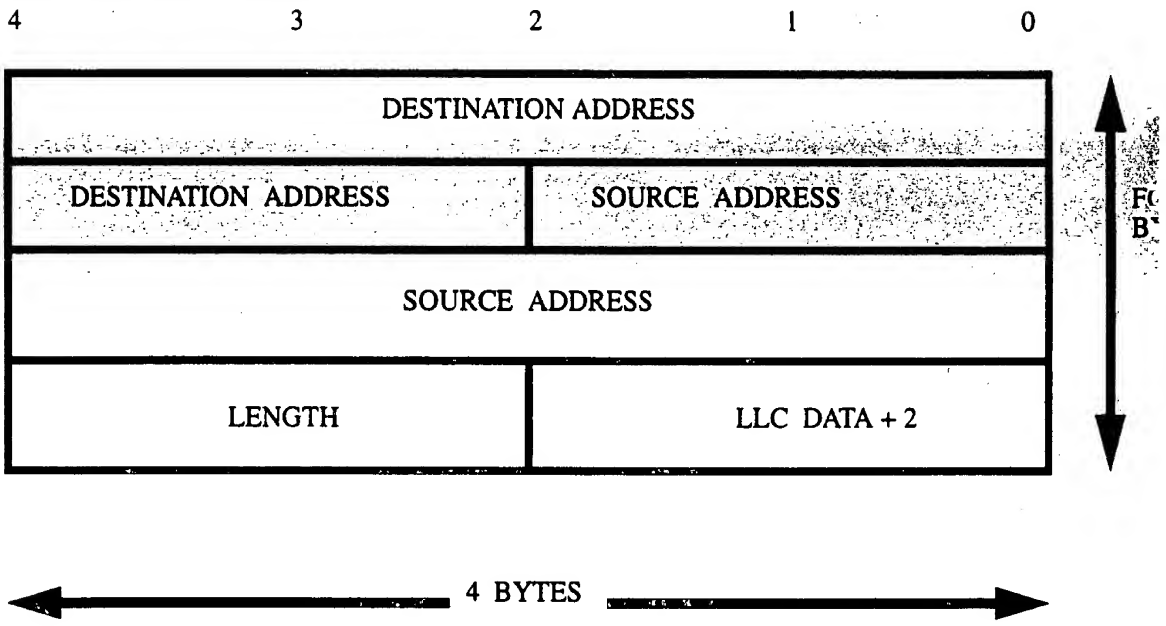
802.3 DATALINK LAYER HEADER (18 Bytes)



File: ~/patents/MAC.HEADER.FM5

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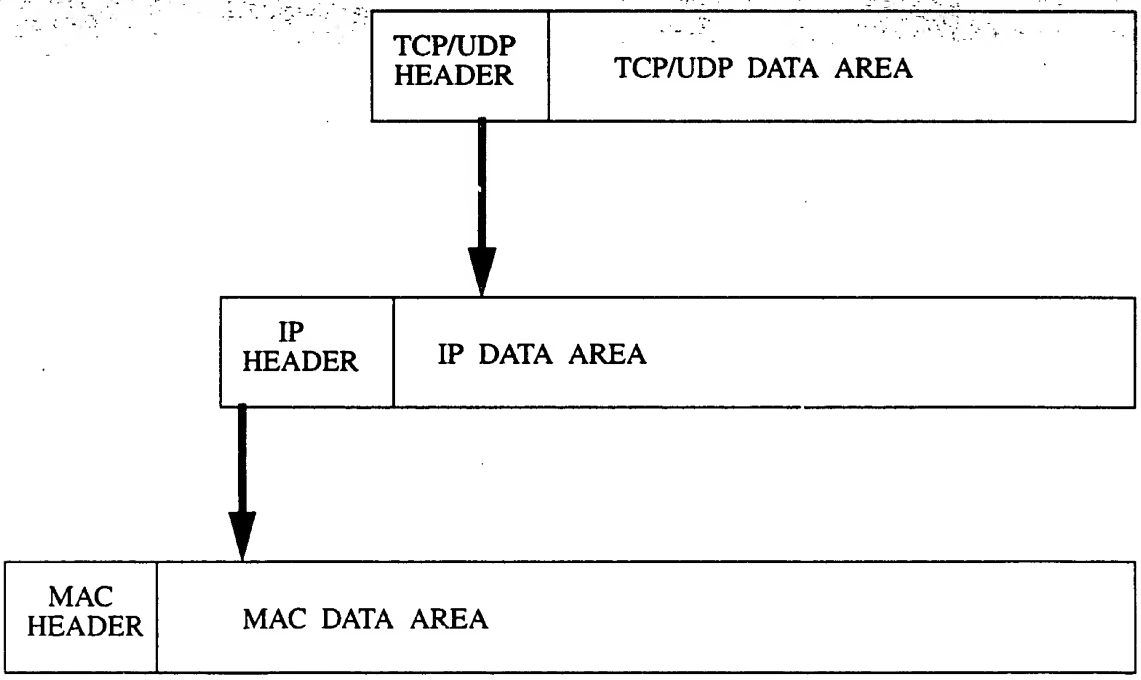
TCP/UDP DATAGRAM ENCAPSULATED IN AN IP AND MAC LAYER FRAME



File: ~/patents/FAN/frames.encap.fm5

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Telephone (214) 466-6000, Telex 730643

From: c.kasper
File: ~/patents/FAN/fan.txt
Date:

Abstract: Signal set to notify the host that the address fields are present in the frame buffer.

Discussion: Frame Address Notification (FAN) is a signal to the host CPU that all relevant address fields for a received frame are currently resident in memory. The frame may then be processed by the address and lookup engine (ALE) and dispatched to its destination. This provides a pipelining effect, if you will, as routing is occurring while the remainder of the frame may still be incoming off the network wire.

In the classic store and forward (SF) architecture, the host device was obligated to wait until the entire frame had been read off the wire and ownership of the associated external memory buffer had been reassigned before routing could take place. As the length of a frame increased then so did the latency of the routing process. Performance became difficult to predict because the host was denied knowledge of the length of incoming frames - even though this information is contained in the header of every frame.

Cut-through (C/T) was implemented as an improvement to the store and forward process. Frames moved from receive ports to transmit ports in constant bursts without ever examing the contents. This expedites movement but at the cost of replicating errored frames across networks. Often enough, due to contention or the convergence of multiple frames to the same destination port, cut-through devolved back into store-and-forward due to the neccessity to buffer waiting frames.

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In addition, careful selection of the DMA burst-size will cause the appropriate address fields to be available. The MAC-level header, IP addresses, or even the TCP/UDP ports will be read into memory depending upon the size of the burst. This lends itself toward L2, L3, or L4 frame switching applications.

In the classic store and forward (SF) architecture, the host device was obligated to wait until the entire frame had been read off the wire and ownership of the associated external memory buffer had been reassigned before routing could take place. As the length of a frame increased then so did the latency of the routing process. Performance became difficult to predict because the host was denied knowledge of the length of incoming frames - even though this information is contained in the header of every frame.

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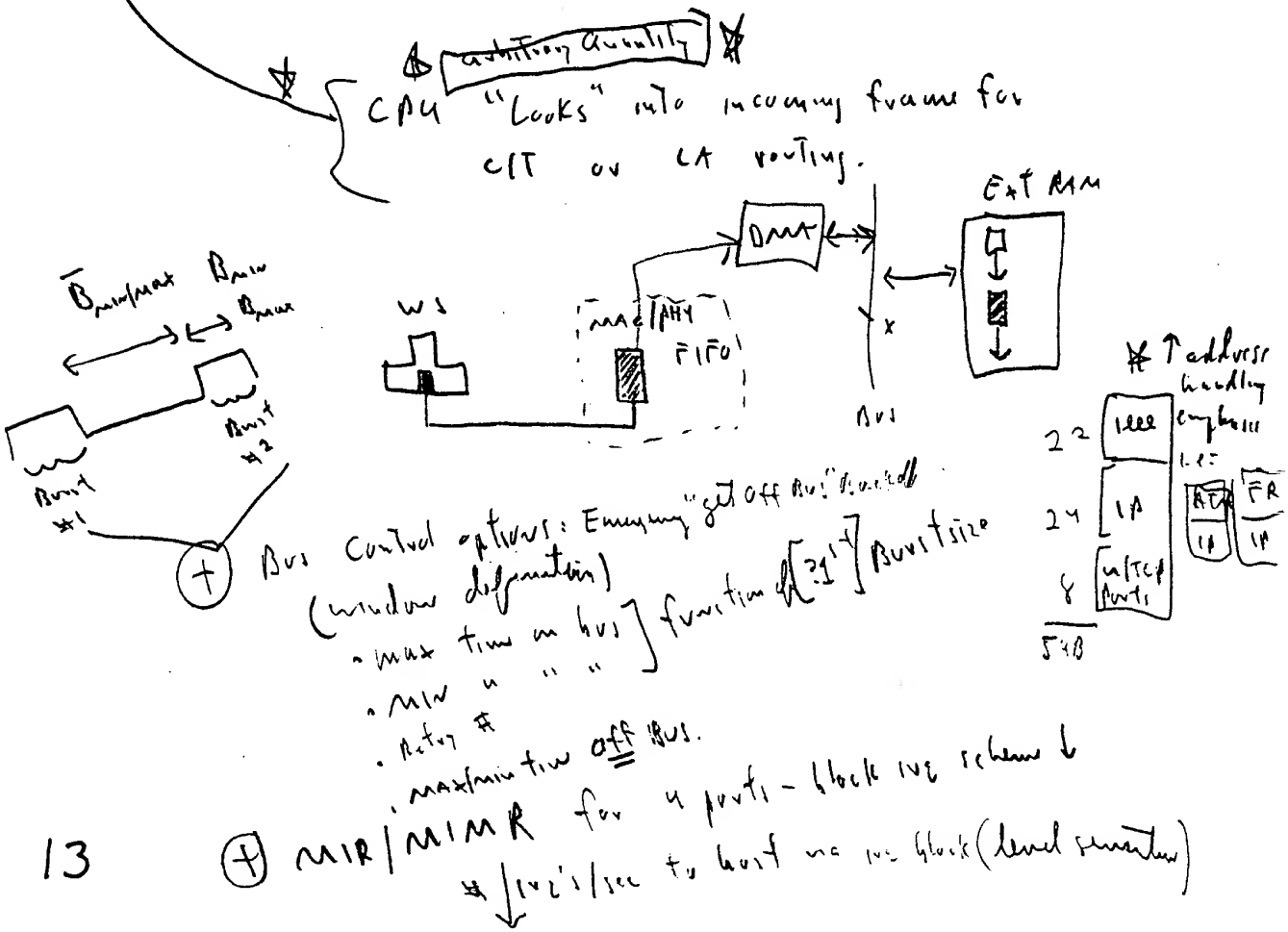


c.kasper
File: ~/patents/FAN/fan.txt
Date:

In a Local Area Network (LAN) system, an ethernet adapter exchanges data with a host through programmed I/O (PIO) and FIFO buffers. The receive PIO emp loys a DMA ring buffer backup so
incoming packets can be copied directly into host memory when the PIO FIFO buffer is full. The adapter may be programmed to generate early receive inte rrupts when only a portion of a packet has
been received from the network, so as to decrease latency. The adapter may also be programmed to generate a second early interrupt so that the copying of a large packet to the host may overlap
reception of the packet end. The adapter to begin packet transmission before the packet is completely transferred from the host to the adapter, which f urther reduces latency. The minimal latency of
the adapter allows it to employ receive and transmit FIFO buffers which are small enough to be contained within RAM internal to an Application Specific Integrated Circuit (ASIC) containing the
transceiver, ethernet controller, FIFO control circuitry and the host interface as well.

Optimized indication signals of a completed data frame transfer are generated by a network adapter which reduces host processor interrupt latency. The network adapter comprises network
interface logic for transferring the data frame between the network and a buffer memory and host interface logic for transferring the data frame betwee n the buffer memory and the host system. The
network adapter further includes threshold logic where a threshold value in an alterable storage location is compared to a data transfer counter in ord er to generate an early indication signal. The
early indication signal may be used to generate an early interrupt signal to a host processor before a transfer of a data frame is completed. The netwo rk adapter also posts status information
status registers which may be used by the host processor to tune the timing of the generation of the network adapter interrupt signal.

Combined indication signals of data block transfers are generated by a device which reduces the number of interrupts to a host processor. The reduction in the number of interrupts enhances host
system performance during data block transfers. An embodiment of the device may be a network adapter comprising network interface logic for transferrin g a data frame between a network and a
buffer memory and host interface logic for transferring a data frame between a buffer memory and a host system. The network adapter further includes th reshold logic for generating an early receive
indication signal when a portion of the data frame is received. Indication combination logic delays the generation of a transfer complete interrupt to slightly before the expected occurrence of the
early receive indication. The host processor is able to service both the transfer complete indication and the early receive indication in a single inte rrupt service routine caused by the transfer
complete indication.

~~store and forward architecture were c~~

Frame Address notification is a signal to the host CPU that all the relevant ~~[illegible]~~ address fields for a frame have been ~~[illegible]~~ received. ~~[illegible]~~ The address may then be processed by the address lookup engine and the frame dispatched to its destination.

In the classic store n forward arch the host was obligated to wait until the entire frame had been received and ownership of the associated buffer assigned to him before routing could take place.

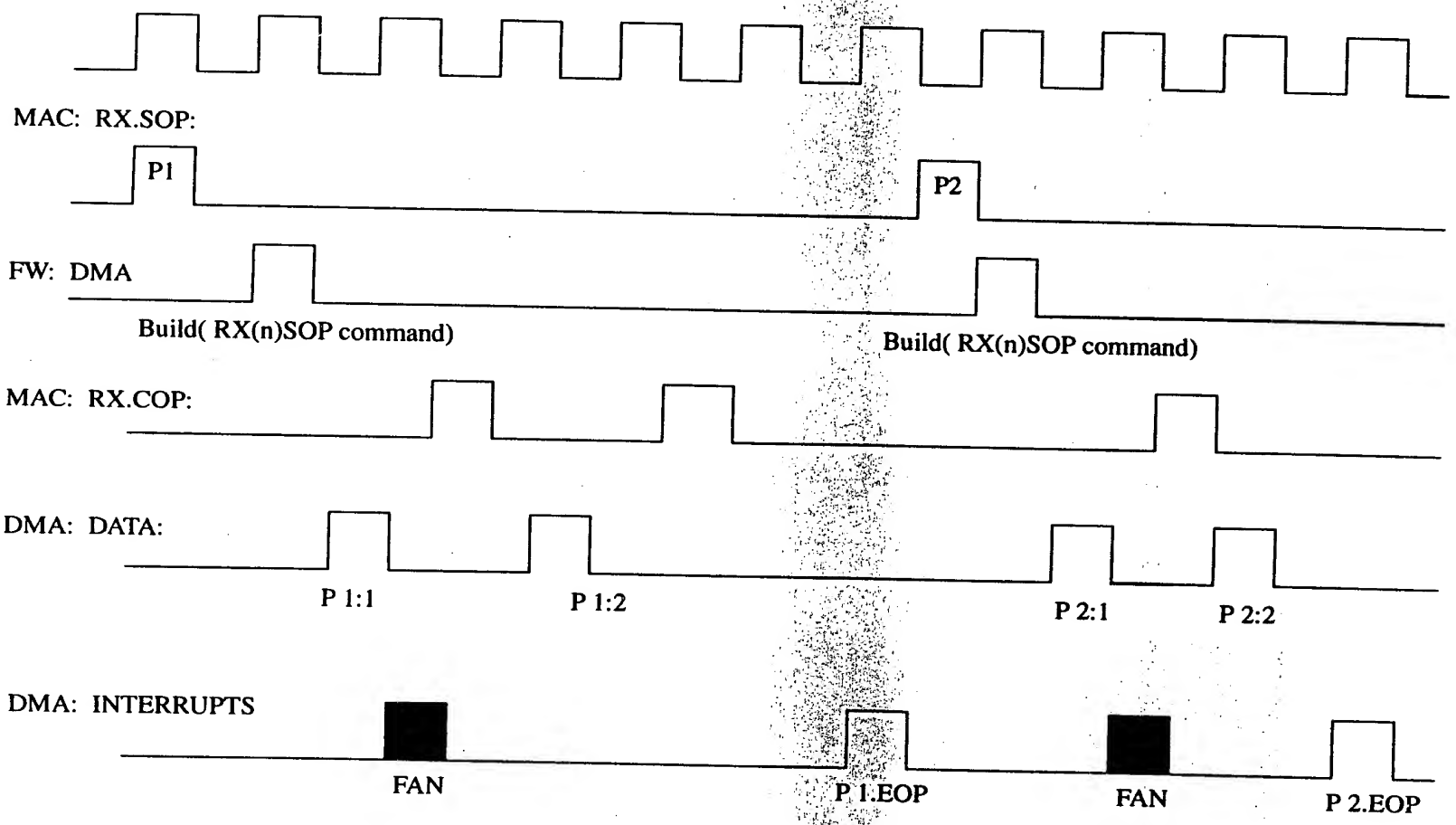
as an improvement cut thru arch were deployed to encourage frame movement. (define). Unfortunately C/T was somewhat problematic in that it replicates errored frames across networks and often, due to (contention / convergence) at destination ports functioned for all intents & purposes identically to S/F

14

RECEIVE INTERRUPT EVENT TIMELINE

15

FRAME ADDRESS NOTIFICATION (FAN)



~/FAN/LanceLot.fsmCycles.RX.fm

SGS-THOMSON MICROELECTRONICS

ST52T3

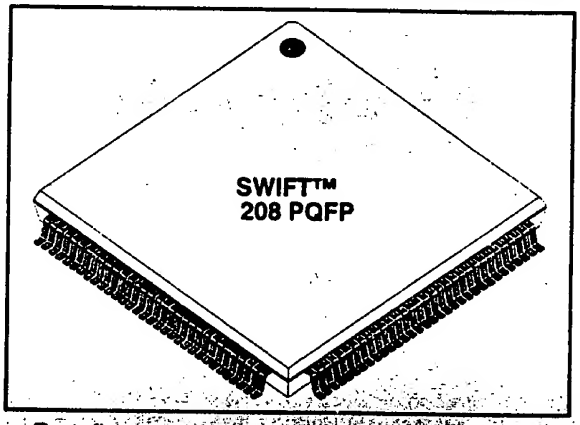
SWIFT™

4-PORT • 32-BIT • Fast HDLC CONTROLLER

PRELIMINARY

FEATURES

- STS-1, T3/E3 Data Rate Compatible
- 262 Mbit/sec maximum HDLC bandwidth:
  - Port 0,1: full-duplex up to 51Mbps each
  - Port 2, 3: full-duplex up to 2Mbps each
- 25-33 MHz system clock speed
- Four on-chip HDLC transmit and receiver:
  - ISO 3309 HDLC compliant
  - ITU V.35 handshake compatible
  - Full/half-duplex operation
  - Separate receive and transmit FIFOs
    - → Two 512-byte FIFOs per port
  - Per-port programmable FIFO watermarks
  - Programmable Transmit FIFO hold-off watermark (TSTART)
  - Handles all HDLC frame formatting:
    - → Zero bit insertion and deletion
    - → FCS (CRC) generation and detection
    - → Frame delimiting with flags
    - → Abort or Idle detection and generation
    - → Interframe fill with Flags or Idle
  - Programmable minimum frame spacing on transmission (number of flags between frames)
    - → Programmable from 0 to 63 flags between frames.
  - Dynamic FCS generation on transmission
  - Two selectable FCS(CRC) polynomials: CRC-16 and CRC-32 bits
  - The entire FCS is passed to buffer
  - CRC can be separately disabled for transmit and receive
- Testing Facilities per port:
  - Internal Loopback
  - Remote Loopback
  - Silent Loopback
  - Optional Internal Data Clock Generation
  - Self Test
  - Selectable Scan Test
- Programmable Watchdog Timers for RCLK and TCLK (to detect absence of data clocks) per port



- Part, firmware, hardware revision number identification via host software interrogation
- Host memory buffer management includes:
  - Look-ahead frame address notification
  - Variable descriptor ring size (0 - 8K)
  - Data buffer chaining for scatter/gather
  - Programmable burst sizes per FIFO
  - Automatic descriptor ring construction
- DMA Features:
  - Maximum transfer rate of 133 Mbytes/sec
  - Single clock 32 bit transfers
  - Non-word aligned byte transfers
  - Selectable Big/Little Endian
  - 32 bit bus interface
- Built-in 32-bit RISC processor for:
  - Buffer management algorithm
  - On-chip statistics maintenance
- Dual supply CMOS; 5V I/O; 3.3V internal logic

APPLICATIONS

- Multiport Frame Relay at T3 rates
- Bridges/routers for up to 51Mbps applications
- Multiport X.25, ISDN LAPD, X.32 and X.75
- Any point-to-point HDLC connections requiring High Speed and Multiple ports

Data Sheet Version 1.1